REMARKS

Claims 1-23, 25, 26, and 28-37 are pending. Claims 20, 23, and 26 have been amended, claims 24 and 27 have been canceled, and new claims 31-37 have been added to recite additional features of the embodiments disclosed in the specification.

In the Office Action, claims 1-30 were rejected under 35 USC § 102(e) for being anticipated by the Mukherjee patent. This rejection is traversed for the following reasons.

Claim 1 recites a clock generator which generates a number of clock signals to control sampling of a data stream. The clock signals are generated to have equally spaced phases, where the equally spaced phases are "determined by a predetermined fraction of a data rate frequency of a data stream." The Mukherjee patent does not disclose these features.

The Mukherjee patent discloses a signal generator 200 that generates a plurality of clock signals (S0, S1, . . . Sn-1) having equal spacing in terms of their phases. The clock signals are input into a detector 205 to control sampling of a data signal 125. (See Fig. 2). However, unlike claim 1, the Mukherjee patent does not disclose or suggest that the equally spaced phases of clock signals (S0, S1, . . . Sn-1) are determined by a predetermined fraction of a data rate frequency **of the data stream** 125.

Contrary to claim 1, the clock signals in Mukherjee are generated using a phase-locked loop (PLL) circuit, which compares a clock signal output from a destination clock 145 with a fed back frequency output from a voltage-controlled oscillator of the PLL. (See Fig. 4). These differences between claim 1 and Mukherjee are further evident from Figure 2, which shows that data stream 125 is only input into detector 205 which operates as the sampler in the Mukherjee circuit, i.e., data stream is not input into destination clock 145 or signal generator 200, and therefore it is evident that clock signals (S0, S1, . . . Sn-1) are not generated based on a data rate frequency of the data stream, as required by claim 1.

Because the Mukherjee patent does not disclose all the features of claim 1, Mukherjee cannot anticipate this claim or any of its dependent claims.

Dependent claim 5 recites that each sampler "samples the data stream based on a different pair of the clock signals." The Mukherjee patent does not disclose or suggest these features. As shown in Fig. 2, detector 205 samples data stream 125 based on the clock signals output from signal generator 200. However, the detector does not include a plurality of samplers, where each sampler samples the data stream based on a different pair of the clock signals. Rather, as shown in Fig. 5, detector 205 includes a plurality of samplers in the form of flip-flop circuits 400a - 400n. Each flip-flop generates a corresponding one of data samples VL0, VL1, . . . VLn based on one and only one clock signal S0, S1, . . . Sn. (See column 6, lines 8-9). Accordingly, the Mukherjee patent does not disclose or suggest the features recited in claim 5.

Dependent claim 7 recites that "the number of samplers and the number of clock signal phases generated by the clock generator are different." The Mukherjee patent does not disclose these features. Each sampler in the Mukherjee circuit is a flip-flop 400. As shown in Fig. 5, the number of flip-flops and the number of phases generated by the clock generator are the same, e.g., there are n flip-flops and clock signals with n phases. Accordingly, the Mukherjee patent does not disclose or suggest the features recited in claim 7.

Dependent claim 8 recites that each sampler samples the data stream "based on a different pair of clock signals having consecutive phases." As shown in Fig. 5, each sampler in the Mukherjee circuit is a flip-flop 400, which samples data stream 125 based on one and only one clock signal. Accordingly, the Mukherjee patent does not disclose or suggest the features recited in claim 8.

Dependent claim 9 recites that the equal spacing of the clock signal phases corresponds to "a symbol duration of the data stream." The Mukherjee patent does not disclose or suggest these features. As shown in Fig. 2, signal generator 200 does not generate the phases of clock signals S0, S1, . . ., Sn based on any attribute of data stream 125, including the symbol duration of this stream, but rather on a phase-locked loop comparison of a destination clock signal 145. Accordingly, claim 9 is allowable over Mukherjee.

Dependent claim 10 recites that the sampling unit "samples the electrical data stream based on the clock signals." The Mukherjee patent does not disclose these features.

Claim 12 recites features similar to those which patentably distinguish claim 1 from the Mukherjee patent. For example, claim 12 recites generating a number of clock signals having equally spaced phases, where each of the phases are "determined by a predetermined fraction of a data rate frequency of a data stream." The Mukherjee patent does not disclose these features.

Claim 23 recites a sampling stage to sample data based on clock signals having different phases, wherein "the difference between the phases of the clock signals at least substantially equals a symbol duration of the data."

The Mukherjee patent discloses generating clock signals having equally spaced phases. However, Mukherjee does not disclose or suggest that the equal spacing between those phases at least substantially equals a symbol duration of the data stream. Rather, the equally spaced phases of the clock signals output from generator 200 are generated by phase-locked loop 200a, which generates the phases based on a comparison of the destination clock signal 145 and a fed back frequency signal output from VCO 315. (See Fig. 4 with reference to column 5, lines 38-52). Applicants submit that claim 23 and its dependent claims are allowable based on these differences.

Claim 26 recites features similar to those which patentably distinguish claim 23 from the Mukherjee patent. Applicants therefore submit that claim 26 and its dependent claims are also allowable.

Claim 29 recites a clock generator to generate a number of clock signals having equally spaced phases "determined by a predetermined fraction of a data rate frequency of a data stream." The Mukherjee patent does not disclose these features. Applicants therefore submit that claim 29 and its dependent claim are allowable.

New claims 31-37 have been added to the application.

Claim 31 recites that the samplers in claim 4 sample the data stream "based on sampling signals that are generated by different pairs of the clock signals." (See, for example, Figures 1-4 for support). The Mukherjee patent does not disclose these features.

Claim 32 recites that consecutive pairs of the clock signals "share a common clock signal." (See, for example, Figures 1-4 for support). The Mukherjee patent does not disclose these features.

Claim 33 recites that "the clock signals in each pair have consecutive phases." (See, for example, Figures 1-4 for support). The Mukherjee patent does not disclose these features.

Claim 34 recites that "the sampling signals having non-overlapping duty cycles." (See, for example, pages 6 and 7 of the specification with reference to Figure 3). The Mukherjee patent does not disclose these features.

Claim 35 recites that "the sampling signals have overlapping duty cycles." (See, for example, page 7 of the specification with reference to Figure 4). The Mukherjee patent does not disclose these features.

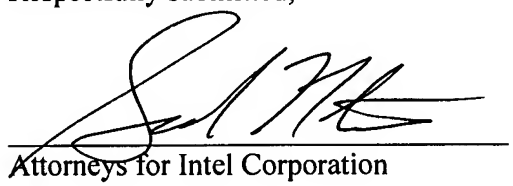
Claim 36 recites that "the clock signals in each pair define different edges of corresponding ones of the sampling signals." (See, for example, Figures 1-4 for support). The Mukherjee patent does not disclose these features.

Claim 37 recites that "the sampling signals have duty cycles which are substantially different from 50%." (See, for example, page 7 for support). The Mukherjee patent does not disclose these features.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of the application is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with this application to Deposit Account No. 16-0607 and credit any excess fees to the same Deposit Account.

Respectfully submitted,



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